Claims 1 through 6 were rejected under 35 U.S.C. §103 for obviousness predicated upon Hembree in view of Tao et al.

In the statement of the rejection, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify Hembree's semiconductor device by providing external connections in view of Tao et al. This rejection is traversed.

Amended claim 1 recites that the heat sink plate is so formed that the convex portions do not protrude from the surface of the sealing member to the outside. This feature is neither disclosed nor suggested by the applied prior art. Indeed, on page 3 of the April 10, 2002 Office Action, in treating claim 4, the Examiner asserts that Hembree discloses a structure wherein "....the heat sink is formed so that the convex portions protrude from the surface of the sealing member to the outside." Ergo, even **if** the applied references are combined as suggested by the Examiner, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).*

Further, Applicant would note that the above argued difference between the claimed invention and the applied prior art is functionally significant. By forming the heat sink plate so that the convex portions do not protrude from the surface of the sealing member to the outside, the entire semiconductor device can be reduced in size. Further, a tray and final test socket used for a semiconductor device which does not have a heat sink plate can also be used for the semiconductor device of claim 1, thereby reducing manufacturing costs. Another advantage is that the heat sink plate can be attached at the same time of processing the molding resins without any special process for attaching the heat sink plate. thereby increasing manufacturing throughput.

There is no apparent factual basis upon which to predicate the conclusion that one having ordinary skill in the art would have been realistically motivated to modify whatever semiconductor device can be said to have been reasonably suggested by the combined disclosures of Hembree and Tao et al. to arrive at the claimed invention. *In re Lee, __F.3d__, 61 USQP2d 1430, (Fed. Cir. 2002).* Applicant, therefore, submits that the imposed rejection of claims 1 through 6 under 35 U.S.C. §103 for obviousness predicated upon Hembree in view of Tao et al. is not factually or legally viable and, hence, solicits withdrawal thereof.

Claims 7 and 10 were rejected under 35 U.S.C. §103 for obviousness predicated upon Schneider in view of Tao et al.

This rejection is traversed. Indeed, this rejection has been rendered moot by incorporating the limitations of claim 8 into claim 7, claim 8 not being subject to this rejection. Clearly, neither Schneider et al. nor Tao et al., taken singly or in combination, disclose or suggest a semiconductor device as defined in claim 7 comprising, inter alia, engaging portions respectively formed on the heat sink plate and the heat dissipation fin to allow detachment of the heat dissipation fin from the heat sink plate.

Applicant, therefore, submits that the imposed rejection of claim 7 and 10 under 35 U.S.C. §103 for obviousness predicated upon Schneider et al. in view of Tao et al. It is not factually or legally viable and, hence, solicits withdrawal thereof.

Claims 8, 9, 11 and 12 were rejected under 35 U.S.C. §103 for obviousness predicated upon Schneider et al. in view of Tao et al. and Suzuki et al.

In the statement of the rejection, the Examiner concluded that the claimed invention would have been obviousness based upon the teachings of Suzuki et al. with respect to an IC card slot 1 and socket 2 having engaging portions. This rejection is traversed as factually and legally erroneous.

Initially, Applicant would treat this rejection as though applied against claim 7, since the limitations of claim 8 has been incorporated into claim 7, with claims, 11 and 12 dependent thereon.

Insufficient Facts

In rejecting a claim under 35 U.S.C. §103, the Examiner is required to identify a **source** in the applied prior art for each claim limitation and for the requisite motivational element. *Smiths Industries Medical System v. Vital Signs Inc., 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999).* Indeed, the Examiner is required to point to "page and line" of a reference wherein a claim limitation is asserted to reside. *In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993).* That burden has not been discharged.

Specifically, the Examiner addresses the claim requirement for engaging portions between the heat sink plate and heat dissipation film by merely identifying an IC card slot 1 and a socket 2 having engaging portions brought into engagement with each other. This is nothing more than, as the Examiner acknowledges, a guide rail for guiding an IC card. The relevance of that evulgation to the claimed invention is not apparent. In short, the guide rail identified by the Examiner for guiding an IC card is **not**, repeat **not**, remotely related to the requirements of claim 7 (previously in claim 8) for a heat sink

plate and heat dissipation fin having respective engaging portions which allow detachment of the heat dissipation fin from the heat sink plate.

The additional references to Schneider et al. and Tao et al., do not cure the argued deficiencies of Suzuki et al. Accordingly, even if all of the applied references are somehow combined, the claimed invention would not result. *Uniroyal Inc. v. Rudkin-Wiley Corp., supra.*

There is no Motivation

The record devoid of any factual basis upon which to predicate the conclusion that one having ordinary skill in the art would have been realistically motivated to modify whatever semiconductor device can be said to have been reasonably generated by the combined disclosures of Schneider et al. and Tao et al. to arrive at the claimed invention. *In re Lee, supra.*

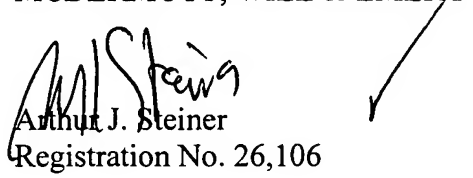
Applicant, therefore, submits that the imposed rejection of claims 8 (7), 9, 11 through 12 under 35 U.S.C. §103 for obviousness predicated upon Schneider et al. in view of Tao et al. and Suzuki et al. is not factually or legally viable and, hence, solicit withdrawal thereof. Applicants further submit that independent claim 7 is free of the applied prior art for reasons argued in traversing this rejection.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 AJS:ntb
Date: July 10, 2002
Facsimile: (202) 756-8087

APPENDIX

Claims 1, 7, 9 and 12 now read as follows.

1. (Amended) A semiconductor device comprising:

a substrate;

a semiconductor chip mounted on the substrate;

external electrodes provided on the back of the substrate, for connecting electrodes of the semiconductor chip to the outside;

a sealing member encapsulating the semiconductor chip on the substrate; and

a heat sink plate fixed by the sealing member, wherein

the heat sink plate has concavo-convex portions formed on an exposed surface thereof and is disposed to make direct contact with a main surface on which semiconductor elements of the semiconductor chip are formed; and

the heat sink plate is so formed that the convex portions do not protrude from the surface of the sealing member to the outside.

4. (Amended) The semiconductor device according to claim 1, wherein the heat sink plate is formed so that the convex portions do not protrude from the surface of the sealing member to the outside.

7. (Amended) A semiconductor device, comprising:

a substrate;

a semiconductor chip mounted on the substrate;

external electrodes provided on the back of the substrate, for connecting electrodes of the semiconductor chip to the outside;

a sealing member for encapsulating the semiconductor chip on the substrate; and

a heat sink plate fixed by the sealing member, wherein

the heat sink plate has a heat dissipation fin formed integrally therewith wherein the heat sink plate and the heat dissipation fin have engaging portions brought into engagement with each other, whereby he engaging portions allow detachment of the heat dissipation fin from the heat sink plate.

9. (Amended) The semiconductor device according to claim 7, wherein the engaging portions are respectively formed at the heat sink plate and the heat dissipation fin and comprise a screw and a threaded hole brought into engagement with each other.

12. (Amended) The semiconductor device according to claim 10, wherein the engaging portions are respectively formed at the heat sink plate and the heat dissipation fin and comprise a screw and a threaded hole brought into engagement with each other.

Claims 2, 4, 6, 8 and 11 have been cancelled.